**WHAT IS CLAIMED IS:**

1. A microprocessor, comprising:

at least one logic circuit;

a selection device coupled to the at least one logic circuit, the selection device providing switching of on/off states of the at least one logic circuit based on a stored logical value; and

a program instruction which sets the stored logical value to control the on/off states of the at least one logic circuit based on anticipated usage of the at least one logical circuit in accordance with an instruction sequence of the microprocessor.

2. The microprocessor as recited in claim 1, wherein the selection device includes a switch which provides a connection from a supply voltage to a power line of the at least one logic circuit in an on state.

3. The microprocessor as recited in claim 1, wherein the selection device includes a switch which provides a connection from ground to a power line of the at least one logic circuit in an on state.

4. The microprocessor as recited in claim 1, further comprising a register coupled to the selection device to store the stored logic value.

5. The microprocessor as recited in claim 4, wherein the register is updated after a number of instruction cycles.

6. The microprocessor as recited in claim 1, further comprising an input table including an instruction sequence and associated resource needs for the at least one logical unit wherein the anticipated usage is determined in accordance with the input table.

7. The microprocessor as recited in claim 1, wherein the anticipated usage of the at least one logical unit includes usage of the at least one logical device after a number of instruction cycles.

8. The microprocessor as recited in claim 1, further comprising an output table including logical states corresponding to power-saving on/off states of the at least one logical device and the program instruction sets the

stored logical value to control the at least one logic circuit in accordance with the power-saving on/off states.

9. A microprocessor, comprising:

a plurality of logic circuits divided into functional groups;

a selection device coupled to each of the functional groups, each selection device providing switching of on/off states of the corresponding functional group based on logical values stored in a register;

a program instruction which sets the logical values in the register to control the on/off states of the functional groups; and

a compiler program which generates the logical values to be set in the register based on instruction sequences which anticipate usage of each of the functional groups.

10. The microprocessor as recited in claim 9, wherein the selection devices each include a switch which provides a connection from a supply voltage to a power line of the functional group in an on state.

11. The microprocessor as recited in claim 9, wherein the selection devices each include a switch which provides a connection from ground to a power line of the functional group in an on state.

12. The microprocessor as recited in claim 9, wherein the register includes one memory location for each functional group.

13. The microprocessor as recited in claim 9, wherein the register is updated after a number of instruction cycles.

14. The microprocessor as recited in claim 9, further comprising an input table generated by the compiler program and including an instruction sequence and associated resource needs for the each of the functional groups wherein the usage of the functional groups is determined in accordance with the input table.

15. The microprocessor as recited in claim 9, wherein the usage of the functional groups includes usage of the functional groups after a number of instruction cycles.

16. The microprocessor as recited in claim 9, further comprising an output table including logical states corresponding to power-saving on/off states of the functional groups.

17. A method for generating embedded instruction sequences to control power to logic circuits in a microprocessor, comprising the steps of:

generating an instruction sequence which controls a functional program for the microprocessor;

analyzing the instruction sequence to determine which of the logic circuits are active on each instruction cycle;

comparing a number of instruction cycles for which each logic circuit will be inactive after a current instruction cycle to a value for each instruction cycle of the functional program; and

inserting instruction sequences to turn each of the logical circuits on or off based on the comparing step.

18. The method as recited in claim 17, wherein the step of inserting instruction sequences include programming

a register with logical values wherein each of the logical circuits are turned on or off based on the logical values.

19. The method as recited in claim 17, wherein the value of the comparing step includes a number determined to provide net power savings in the logical circuits.

20. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps as recited in claim 17.